a second gate electrode formed on said second gate insulation film, and

a second side insulation film formed at least on side of said second gate insulation film and having said second relative permittvity,

wherein, when a cross-section on a side of said first channel is S1, a cross-section on a side of said first gate electrode is S2, a cross-section on a side of said second channel is S3, and a cross-section on a side of said second gate insulation film is S4, a condition of:

$$S2/S1 > S4/S3$$

is satisfied, and

an area of a bottom part of said first gate electrode in contact with the first gate insulation film is larger than an area of an upper part of said first gate insulation film, and an area of a bottom part of said second gate electrode in contact with the second gate insulation film is larger than an area of an upper part of said second gate insulation film.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-12 are presently active in this application. Claims 1, 6, 9, and 10 have been amended.

In the outstanding Office Action, the title of the invention was objected to for not being descriptive. Claims 1-12 were rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification.[3] Claims 1, 2, and 4-9 were rejected under 35 U.S.C. §102(e) as being anticipated by Krivokapic et al. (U.S. Pat.

[3]Applicants interpret this rejection in light of the specific identifications of indefiniteness listed after the stated 35 U.S.C. §112, first paragraph, rejection.

No. 6,100,598). Claims 3, 10 and 11 were rejected under 35 U.S.C.§103(a) as being unpatentable over Krivokapic et al. (U.S. Pat. No. 6,100,598). Claim 12 was indicated as being allowable if rewritten to overcome the rejection(s) under 35 U.S.C. §112 set forth in the outstanding Office Action and to include all of the limitations of the base claim and any intervening claims.

Regarding the 35 U.S.C. §112 rejection, the specific identifications of indefiniteness listed in the outstanding Office Action have been addressed in the claim amendments. The phrases "assuming" and "is assumed" have been removed from Claim 1. Further, Claim 1 has been amended to define that the first area S_1 is adjacent to the gate electrode and the second area S_2 is adjacent to the channel. Claim 6 has been amended to remove the reference to "the predetermined distance"originally in Claim 6. Claim 9 has been amended to clarify that an electric flux density in the gate insulation film on a side towards the channel side is more dense than an electric flux density in the gate insulation film on a side towards the gate electrode. Hence, it is respectfully submitted that the specific identifications of indefiniteness listed in the 35 U.S.C. §112 rejection have been overcome.

Independent Claims 1, 9, and 10 have been amended, without adding new matter, to define semiconductor devices in which an area of a bottom part of a gate electrode in contact with the gate insulation film is larger than an area of an upper part of the gate insulation film. This feature is shown in Applicants' Figures 11C, 13G, 14C, 22H, and 24H which show that the width of gate electrode 15 at its contact with the gate insulation film 14 is larger than the width of the gate insulation film 14. With this configuration, not only the channel region(s) of the semiconductor devices defined Claims 1, 9, and 10, but also the source, drain, element isolation, and gate contacting regions can be widened as shown in comparison Applicants' Figure 12C with Applicants' prior art Figure 12A.

In the gate electrode shown in Krivokapic et al., since the gate electrode is embedded in a Damascene trench (i.e. the trench established by the sidewalls of the polysilicon spacers 194 and 196), the width of the gate electrode in contact with the gate insulation film (i.e the width of the gate metal layer 220 in contact with the gate oxide 210) is constrained by the polysilicon spacers 194 and 196. Thus, the feature of an area of a bottom part of a gate electrode in contact with the gate insulation film being larger than an area of an upper part of a gate insulation film is not disclosed or suggested in Krivokapic et al.

Furthermore, while the gate structure in Krivokapic et al. concentrates electric flux, the width of the gate electrode cannot be adjusted, and the resistance of the gate increases as the trench dimensions decrease. Accordingly, device performance in Krivokapic et al. cannot be improved. In contrast, as shown in Figures 13G, 14C, 22H, and 24H, since the width of the gate electrode can be substantially larger than the gate insulation film, Applicants submit that a proper resistance for the gate electrode can be obtained, thereby achieving a high-performance transistor.

With Krivokapic et al. not disclosing or suggesting an area of a bottom part of a gate electrode in contact with the gate insulation film being larger than an area of an upper part of the gate insulation film, as defined in Claims 1, 9, and 10, it is respectfully submitted that Claims 1, 9, and 10 and Claims 2-8 which depend from Claim 1 and Claims 11-12 which depend from Claim 10 patentably define over the applied prior art.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Registration No. 25,599
Eckhard H. Kuesters
Attorneys of Record
Registration No. 28,870

Robert T. Pous
Registration No. 29,099

22850

(703) 413-3000
Fax #: (703) 413-2220
GJM:EHK:RAR:clh
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Serial No: 09/340,720
Amendment Filed on: 2/15/2002

IN THE TITLE

Please amend the title on page 1, line 1, as follows:

[SEMICONDUCTOR DEVICE] MOSFET HAVING HIGH AND LOW DIELECTRIC MATERIALS

IN THE CLAIMS

Please amend the Claims as follows:

1. (Amended) A semiconductor device comprising:

a channel of a first [conductive] conductivity type formed on a surface layer of a semiconductor substrate;

a source and a drain of a second [conductive] conductivity type formed on both sides of the channel;

a gate insulation film with a first relative permittivity formed at least on said channel directly or through a buffer insulation film;

a gate electrode formed on said gate insulation film; and

a side insulation film formed at least on a side of said gate insulation film and having a second relative permittivity which is smaller than the first relative permittivity, wherein

when [assuming that an] a first area of said gate insulation film, [which is] the first area being adjacent to said [surface layer on a] gate electrode [side], is S_1, and [an] a second area thereof, [which is] the second area being adjacent to [said surface layer on] said channel

[side], is S2, the area S1 is larger than the area S2, and an area of a bottom part of said gate electrode in contact with the gate insulation film is larger than S1.

6. (Amended) The semiconductor device according to Claim 1, wherein a sectional shape [along a direction of the source-drain] of said gate insulation film along a direction from the gate electrode to said channel [the predetermined distance is a rectangle, and] is one of a tapered shape, a trapezoid, a sector, and a stair [on channel side therefrom].

9. (Amended) A semiconductor device comprising:

a channel of a first [conductive] conductivity type formed on a surface layer of a semiconductor substrate;

a source and a drain of a second [conductive] conductivity type formed on both sides of the channel;

a gate insulation film with a first relative permittvity formed at least on said channel directly or through a buffer insulation film;

a gate electrode formed on said gate insulation film; and

a side insulation film formed at least on a side of said gate insulation film and having a second relative permittvity which is smaller than the first relative permittivity,

wherein an electric flux density in said gate insulation film on a side towards the channel side is more dense [closer] than [that] an electric flux density in said gate insulation film on a side towards the gate electrode, [side] and an area of a bottom part of said gate electrode in contact with the gate insulation film is larger than an area of an upper part of said gate insulation film.

10. (Amended) A semiconductor device comprising:

a plurality of first MOS [type] transistors, each of said first MOS transistors including, [comprising]

a first channel of a first [conductive] conductivity type formed on a surface layer of a semiconductor substrate,

a first source and a first drain of a second [conductive] conductivity type formed to both sides of said first channel,

a first gate insulation film with a first relative permittivity formed at least on the first channel directly or through a buffer insulation film,

a first gate electrode formed on said first gate insulation film, and

a first side insulation film formed at least on side of said first gate insulation film and having a second relative permittivity which is smaller than the first relative permittvity; and

a plurality of second MOS [type] transistors, each of said second MOS transistors including, [comprising]

a second channel of [a] the first [conductive] conductivity type formed on a surface layer of said substrate,

a second source and a second drain of [a] the second [conductive] conductivity type formed on both sides of said second channel,

a second gate insulation film with the first relative permittvity formed at least on said second channel directly or through a buffer insulation film,

a second gate electrode formed on said second gate insulation film, and

a second side insulation film formed at least on side of said second gate insulation film and having [a] said second relative permittvity [which is smaller than the first relative permittvity],

wherein, when a cross-section on a side of said first channel [side of said first gate insulation film is assumed to be] S1, a cross-section on a side of said first gate electrode [side] is [assumed to be] S2, a cross-section on a side of said second channel [side of said

second gate insulation film is assumed to be] S3, and a cross-section on a side of said second gate insulation film is [assume to be] S4, a condition of:

$$S2/S1 > S4/S3$$

is satisfied,and

an area of a bottom part of said first gate electrode in contact with the first gate insulation film is larger than an area of an upper part of said first gate insulation film, and an area of a bottom part of said second gate electrode in contact with the second gate insulation film is larger than an area of an upper part of said second gate insulation film.